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Basics | Synopsys

VLOG! A few days

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7-20-2010 - Part 2
of 2 Uvm Tips And
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applying certain tips

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and tricks while building UVM test benches, which is mainly the purpose of this article. The

Aim of this Paper:

1. Focus on the common mistakes made by the novice engineers or experienced users while working on UVM Methodology.

2. Tricks to

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enhance the
productivity using
UVM Methodology.

3. Conventions for
using UVM
methodology

features. 4.

Common hierarchy
giving well

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- Logic Fruit

Technologies

2. TRICKS TO

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ENHANCE THE PRODUCTIVITY USING UVM METHODOLOGY

2.1 Avoid using
uvm_config_db for
Replicating the
Changes between
Components. The
"uvm_config_db"
should not be used
to communicate
between different
components of the

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testbench when the number of variables becomes too much. Instead it's better to have a common object.

[UVM Tips and Tricks | Verification Horizons - March 2017 ...](#)
class
serial_sequence

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extends Compile Time

```
uvm_sequence #(serial_transaction);...
```

```
task body; if
```

```
(starting_phase !=  
null) // UVM 1.1 sta
```

```
rtling_phase.raise_o  
bjection(this);
```

```
repeat (count)
```

```
begin @DUT_ready
```

```
`uvm_do( trans )
```

```
end if
```

```
(starting_phase !=  
null) starting_phase
```

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`.drop_objection(this
)`; endtask endclass
: serial_sequence.

Don't put DUT
timing into
sequence

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Learn and then become productive with UVM as quickly as possible and to reduce the burden of supporting UVM code within a company or organization. The Easier UVM Coding Guidelines 2) to compile with Modelsim use the

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makefile.questa . I
would do this copy
makefile.questa as
Makefile .

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This tutorial
delivers a plethora
of tips and tricks to
alleviate the
struggle. It walks
you through an

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introduction of UVM testbench features, includes real-world examples including common errors and fixes, and details how to use the built in debugging features in UVM.

Technical Tutorial:
UVM Tips and
Tricks Plus
Preparing for ...

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4.18 SystemVerilog OVM or UVM Library

Compilation.

Typically the OVM
or UVM libraries
are compiled using
directives like: +inc
dir + /path/to/xvm/src
. /path/to/xvm/src/
xvm_pkg.sv. Using
the -ovm or -uvm
directives. You can
use the - ovm or -

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"-uvm" directives
to compile the OVM
or UVM libraries.

4.18 SystemVerilog OVM or UVM Library Compilation

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Tips and Tricks.

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The following tips and tricks give some helpful ideas for increasing your productivity. ...

Quick Compile Order: You can quickly open a file that is included via the top files. ... then select Refactor > Migrate OVM to UVM. See OVM to UVM Migration

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documentation page
for more details.

Add a new file
extension to
compile list ...

Chapter 42. Tips and Tricks - DVT Eclipse

2) to compile with
Modelsim use the
makefile.questa . I
would do this copy
makefile.questa as

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Makefile . Then do
gmake and it would
be fine . 3)If you

wanted to see the
compile command
do this . gmake -n
> run.csh . chmod
775

run.csh./run.csh [
We are just trying
to make a run script
without any
makefiles] Hope
this works!

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Steps to run an
UVM example? -
UVM Simulator
Specific ...

I downloaded the
uvm package (UVM
1.1 (tar.gz) -
Accellera) from
verification
academy. While
trying to compile
the uvm code +
u_first.sv I see the

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following error.

Compile command
used:-----vlog

-timescale

"1ns/1ns" -mfcu

-suppress 2181 +d

efine+UVM_NO_DP

| +acc=rmb

+incdir+uvm/src

uvm/src/uvm.sv

u_first.sv.

ERROR:-----

Compiling UVM |

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Verification

Academy

UVM / OVM Other

Libraries Enable TL-

Verilog . Enable

Easier UVM .

Enable VUnit .

Libraries Top

entity. Enable VUnit

. Specman ...

Compile Options.

Run Options ...

uvm_re_match - tips

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and tricks - EDA
Playground

2. TRICKS TO
ENHANCE THE
PRODUCTIVITY
USING UVM
METHODOLOGY.

2.1 Avoid using
uvm_config_db for
Replicating the
Changes between
Components. The
“ uvm_config_db ”
should not be used

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to communicate between different components of the testbench when the number of variables becomes too much. Instead it ' s better to have a common object.

UVM Tips and Tricks - Mentor Graphics

Easier UVM is a set

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of vendor-neutral coding guidelines accompanied by a code generator that creates UVM code compliant to those guidelines. Easier UVM was created to help individuals and project teams learn and then become productive with UVM as quickly as possible

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and to reduce the burden of supporting UVM code within a company or organization.

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He will share some of his favorite advanced SystemVerilog knowledge, including OVM and UVM tips and tricks. Topic overview: * New UVM 1.0 overview and comparison to OVM. * Important

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OVM and UVM
phasing. * Secrets
in mastering OVM
and UVM. *

Graceful
termination of tests
in OVM and UVM
with emphasis on
the objection
mechanism.

Cliff Cummings to
present Advanced
SystemVerilog tips

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randomize the item
or sequence. call
the start_item ()
and finish_item () if
its a
uvm_sequence_item
object. call the start
() task if its a
sequence. `uvm_do :
execute this
sequence on default
sequencer with the
item provided.

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``uvm_do_with`:
override any default
constraints with
inline values.

How to use `uvm_do sequence macros

hi, all, Im a newer
in learning UVM.
With the support of
many UVM experts,
we can find many
examples for
learnning UVM.

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However, when I tried to have a taste on some examples using VCS to compile them, the Makefile is a headache for me. Could you please let me know how to write a good Makefile fo...

[How to write a good Makefile in VCS for](#)

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running UVM tests

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Press Shift + Alt +
Down Arrow to
restore the
previous selection
step made with
Shift + Alt + Up
Arrow. Format
source: Use the
Format Source
action from the
editor right click
menu Source >

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Format Source. The whole file is formatted or the current selection, if any. One key indentation: If you press Tab once at the beginning of a line, it is automatically aligned to the enclosing context. Press ...

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